

## Single-Channel, Adjustable Supervisory Circuit in Ultra-Small Package

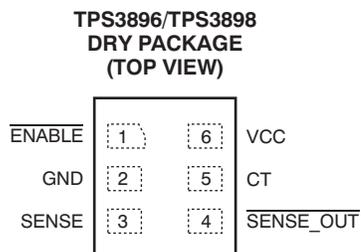
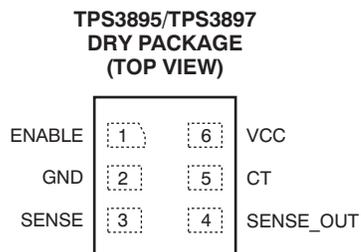
Check for Samples: [TPS3895](#), [TPS3896](#), [TPS3897](#), [TPS3898](#)

### FEATURES

- Very Small  $\mu$ SON (1.5 mm  $\times$  1 mm) Package
- Adjustable Threshold down to 500 mV
- Threshold Accuracy: 1.0% Over Temperature
- Capacitor-Adjustable Delay Time
- Low Quiescent Current: 6  $\mu$ A (typ)
- External Enable Input
- Open-Drain/Push-Pull Output Options
- Temperature Range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

### APPLICATIONS

- DSPs, Microcontrollers, and Microprocessors
- Notebook and Desktop Computers
- PDAs and Handheld Products
- Portable and Battery-Powered Products
- FPGA and ASIC



### DESCRIPTION

The TPS3895, TPS3896, TPS3897, and TPS3898 devices (TPS389x) are a family of very small supervisory circuits that monitor voltage greater than 500 mV with a 0.25% (typical) threshold accuracy and has capacitor-adjustable, delay-time flexibility. The TPS389x family also has a logic enable pin (ENABLE or  $\overline{\text{ENABLE}}$ ) to power on/off the output. With the TPS3895, for example, when the input voltage pin (SENSE) falls below the threshold, or if the enable pin (ENABLE) is low, then the output pin (SENSE\_OUT) goes low. When SENSE rises above the threshold and ENABLE is high, then SENSE\_OUT goes high after the capacitor-adjustable delay time elapses (A version only; for differences between the A and P versions, see [Table 1](#)). For truth tables, see [Table 2](#) and [Table 3](#).

For TPS389xA versions, there is a capacitor-adjustable delay from when the enable pin asserts to when the output pin asserts; this period is the same as the delay from SENSE to the output pin. The TPS389xP devices have a fixed propagation delay from when the enable pin asserts to when the output pin asserts.

All devices operate from 1.8 V to 6.5 V and have a low quiescent current of 6  $\mu$ A with an open-drain output rated at 18 V. The TPS389x is available in an ultra-small  $\mu$ SON package and is fully specified over the temperature range of  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

**Table 1. FAMILY COMPARISON**

DEVICE	ENABLE	OUTPUT	INPUT (SENSE) DELAY	ENABLE DELAY
TPS3895A	Active high	Active high, push-pull	Capacitor adjustable	Capacitor adjustable
TPS3895P	Active high	Active high, push-pull	Capacitor adjustable	150 ns
TPS3896A	Active low	Active low, push-pull	Capacitor adjustable	Capacitor adjustable
TPS3896P	Active low	Active low, push-pull	Capacitor adjustable	150 ns
TPS3897A	Active high	Active high, open-drain	Capacitor adjustable	Capacitor adjustable
TPS3897P	Active high	Active high, open-drain	Capacitor adjustable	150 ns
TPS3898A	Active low	Active low, open-drain	Capacitor adjustable	Capacitor adjustable
TPS3898P	Active low	Active low, open-drain	Capacitor adjustable	150 ns

**PRODUCT PREVIEW**


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	DESCRIPTION
TPS389wxyyyz	<b>w</b> is output configuration (see <a href="#">Table 1</a> ) <b>x</b> is different delay from enable pin (see <a href="#">Table 1</a> ) <b>yyy</b> is package designator <b>z</b> is package quantity

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage <sup>(2)</sup>	VCC	-0.3	7	V
	CT	-0.3	V <sub>CC</sub> + 0.3	V
	ENABLE, SENSE, SENSE_OUT (push-pull)	-0.3	7	V
	SENSE_OUT (open-drain)	-0.3	20	V
Current	SENSE_OUT		±10	mA
Temperature	Operating junction, T <sub>J</sub>	-40	+125	°C
	Storage, T <sub>stg</sub>	-65	+150	°C
Electrostatic discharge rating <sup>(3)</sup>	Human body model (HBM)		2	kV
	Charge device model (CDM)		500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground terminal.

(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

### THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TPS389x	UNITS
		DRY (μSON)	
		6 PINS	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	293.8	°C/W
θ <sub>JCTop</sub>	Junction-to-case (top) thermal resistance	165.1	
θ <sub>JB</sub>	Junction-to-board thermal resistance	160.8	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	27.3	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	65.8	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance	65.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## ELECTRICAL CHARACTERISTICS

Over the operating temperature range of  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $1.7\text{ V} < V_{CC} < 6.5\text{ V}$ , unless otherwise noted. Typical values are at  $T_J = +25^{\circ}\text{C}$  and  $V_{CC} = 3.3\text{ V}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	$T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	1.7		6.5	V
		$T_J = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	1.65		6.5	V
V <sub>(POR)</sub>	Power-on reset voltage <sup>(1)</sup>	$V_{OL}(\text{max}) = 0.2\text{ V}$ , $I_{OL} = 15\ \mu\text{A}$			0.8	V
I <sub>CC</sub>	Supply current (into VCC pin)	$V_{CC} = 3.3\text{ V}$ , no load		6	12	$\mu\text{A}$
		$V_{CC} = 6.5\text{ V}$ , no load		7	12	$\mu\text{A}$
V <sub>IT+</sub>	Positive-going input threshold voltage	$V_{(\text{SENSE})}$ rising	0.495	0.5	0.505	V
V <sub>hys</sub>	Hysteresis voltage	$V_{(\text{SENSE})}$ falling		5		mV
I <sub>(SENSE)</sub>	Input current <sup>(2)</sup>	$V_{(\text{SENSE})} = 0\text{ V}$ or $V_{CC}$	-15		15	nA
I <sub>(CT)</sub>	CT pin charge current		260	310	360	nA
V <sub>(CT)</sub>	CT pin comparator threshold voltage		1.180	1.238	1.299	V
R <sub>(CT)</sub>	CT pin pull-down resistance			200		$\Omega$
V <sub>IL</sub>	Low-level input voltage (ENABLE pin)				0.4	V
V <sub>IH</sub>	High-level input voltage (ENABLE pin)		1.4			V
UVLO	Undervoltage lockout <sup>(3)</sup>	$V_{CC}$ falling	1.4		1.7	V
I <sub>lkg</sub>	Leakage current	ENABLE = $V_{CC}$ or GND	-100		100	nA
V <sub>OL</sub>	Low-level output voltage	$V_{CC} \geq 1.2\text{ V}$ , $I_{\text{SINK}} = 90\ \mu\text{A}$ (TPS3895/7 only)			0.3	V
		$V_{CC} \geq 2.25\text{ V}$ , $I_{\text{SINK}} = 0.5\text{ mA}$			0.3	V
		$V_{CC} \geq 4.5\text{ V}$ , $I_{\text{SINK}} = 1\text{ mA}$			0.4	V
V <sub>OH</sub>	High-level output voltage (push-pull)	$V_{CC} \geq 2.25\text{ V}$ , $I_{\text{SOURCE}} = 0.5\text{ mA}$	$0.8V_{CC}$			V
		$V_{CC} \geq 4.5\text{ V}$ , $I_{\text{SOURCE}} = 1\text{ mA}$	$0.8V_{CC}$			V
I <sub>lkg(OD)</sub>	Open-drain output leakage current	$V_{(\text{SENSE\_OUT})}$ high impedance = 18 V			1	$\mu\text{A}$
t <sub>pd(r)</sub>	SENSE (rising) to SENSE_OUT propagation delay	$V_{(\text{SENSE})}$ rising, $C_{(\text{CT})} = \text{no capacitor}$		40		$\mu\text{s}$
		$V_{(\text{SENSE})}$ rising, $C_{(\text{CT})} = 0.047\ \mu\text{F}$		190		ms
t <sub>pd(f)</sub>	SENSE (falling) to SENSE_OUT propagation delay	$V_{(\text{SENSE})}$ falling		16		$\mu\text{s}$
	Startup delay <sup>(4)</sup>			50		$\mu\text{s}$
t <sub>w</sub>	ENABLE pin minimum pulse duration		1			$\mu\text{s}$
	ENABLE pin glitch rejection			100		ns
t <sub>d(off)</sub>	ENABLE to SENSE_OUT delay time (output disabled)	Output enabled to output disabled delay		150		ns
t <sub>d(P)</sub>	ENABLE to SENSE_OUT delay time (P version)	Output disabled to output enabled delay (P version)		150		ns
t <sub>d(A)</sub>	ENABLE to SENSE_OUT delay time (A version)	Output disabled to output enabled delay (A version), $C_{(\text{CT})} = \text{no capacitor}$		20		$\mu\text{s}$
		Output disabled to output enabled delay (A version), $C_{(\text{CT})} = 0.047\ \mu\text{F}$		190		ms

- (1) The lowest supply voltage ( $V_{CC}$ ) at which output is active ( $\text{SENSE\_OUT}$  is low,  $\overline{\text{SENSE\_OUT}}$  is high);  $t_r(V_{CC}) > 15\ \mu\text{s/V}$ . Below  $V_{(\text{POR})}$ , the output cannot be determined.
- (2) Specified by design.
- (3) When  $V_{CC}$  falls below the UVLO threshold, the output de-asserts ( $\text{SENSE\_OUT}$  goes low,  $\overline{\text{SENSE\_OUT}}$  goes high). Below  $V_{(\text{POR})}$ , the output cannot be determined.
- (4) During power on,  $V_{CC}$  must exceed 1.7 V for at least 50  $\mu\text{s}$  (plus propagation delay time,  $t_{pd(r)}$ ) before output is in the correct state.

### TIMING DIAGRAM

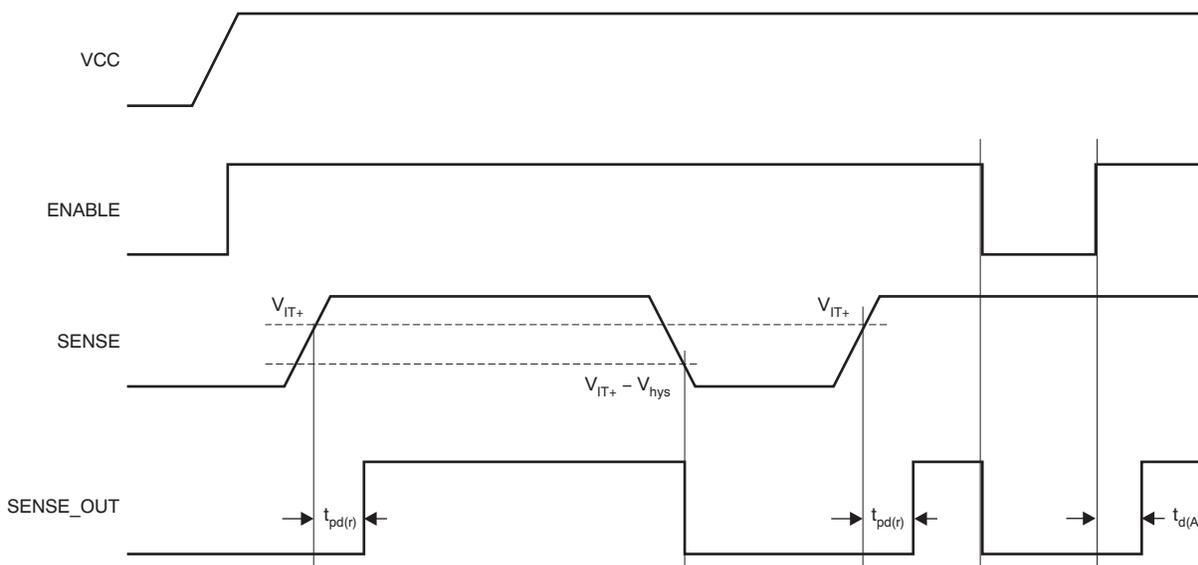


Figure 1. TPS3895A/TPS3897A Timing

Table 2. TPS3895/7 Truth Table

CONDITION	OUTPUT	STATUS
ENABLE = high, SENSE < $V_{IT+}$	SENSE_OUT = low	Output not asserted
ENABLE = low, SENSE < $V_{IT+}$	SENSE_OUT = low	Output not asserted
ENABLE = low, SENSE > $V_{IT+}$	SENSE_OUT = low	Output not asserted
ENABLE = high, SENSE > $V_{IT+}$	SENSE_OUT = high	Output asserted after delay

Table 3. TPS3896/8 Truth Table

CONDITION	OUTPUT	STATUS
$\overline{\text{ENABLE}}$ = low, SENSE < $V_{IT+}$	$\overline{\text{SENSE\_OUT}}$ = high	Output not asserted
$\overline{\text{ENABLE}}$ = high, SENSE < $V_{IT+}$	$\overline{\text{SENSE\_OUT}}$ = high	Output not asserted
$\overline{\text{ENABLE}}$ = high, SENSE > $V_{IT+}$	$\overline{\text{SENSE\_OUT}}$ = high	Output not asserted
$\overline{\text{ENABLE}}$ = low, SENSE > $V_{IT+}$	$\overline{\text{SENSE\_OUT}}$ = low	Output asserted after delay

### TYPICAL APPLICATION

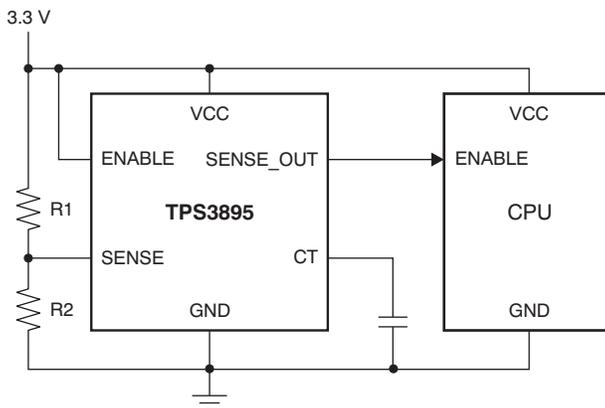
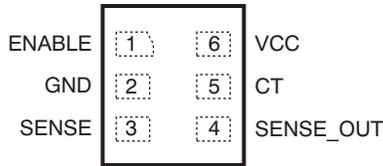


Figure 2. TPS3895 Typical Application

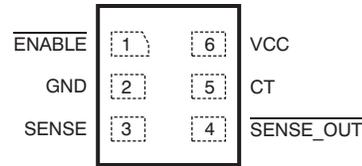
PRODUCT PREVIEW

## PIN CONFIGURATIONS

DRY PACKAGE: TPS3895, TPS3897  
USON-6  
(TOP VIEW)



DRY PACKAGE: TPS3896, TPS3898  
USON-6  
(TOP VIEW)



## PIN ASSIGNMENTS

PIN NAME	TPS3895/ TPS3897	TPS3896/ TPS3898	DESCRIPTION
CT	5	5	Capacitor-adjustable delay. The CT pin offers a user-adjustable delay time. Connecting this pin to a ground referenced capacitor sets the delay time for SENSE rising above 0.5 V to SENSE_OUT (and ENABLE to SENSE_OUT for A version devices). $t_{pd} = (C_{(CT)} \times 4.0 \times 10^9) + 40 \mu s$ .
ENABLE	1	—	Active high input. Driving ENABLE low immediately makes SENSE_OUT go low, independent of $V_{(SENSE)}$ . With $V_{(SENSE)}$ already above $V_{IT+}$ , drive ENABLE high to make SENSE_OUT go high after the capacitor-adjustable delay time (A version) or the fixed time (P version).
$\overline{ENABLE}$	—	1	Active low input. Driving $\overline{ENABLE}$ high immediately makes $\overline{SENSE\_OUT}$ go high, independent of $V_{(SENSE)}$ . With $V_{(SENSE)}$ already above $V_{IT+}$ , drive $\overline{ENABLE}$ low to make SENSE_OUT go low after the capacitor-adjustable delay time (A version) or the fixed time (P version).
GND	2	2	Ground
SENSE	3	3	This pin is connected to the voltage that is monitored with the use of external resistor. The output asserts after the capacitor-adjustable delay time when $V_{(SENSE)}$ rises above 0.5 V and ENABLE is asserted. The output de-asserts immediately when $V_{(SENSE)}$ falls below $V_{IT+} - V_{hys}$ .
SENSE_OUT	4	—	SENSE_OUT is an open-drain/push-pull output that is immediately driven low after $V_{(SENSE)}$ falls below $V_{IT+} - V_{hys}$ or the ENABLE input is low. SENSE_OUT goes high after the capacitor-adjustable delay time when $V_{(SENSE)}$ is greater than $V_{IT+}$ and the ENABLE pin is high.
$\overline{SENSE\_OUT}$	—	4	$\overline{SENSE\_OUT}$ is an open-drain/push-pull output that is immediately driven high after $V_{(SENSE)}$ falls below $V_{IT+} - V_{hys}$ or the $\overline{ENABLE}$ input is high. $\overline{SENSE\_OUT}$ goes low after the capacitor-adjustable delay time when $V_{(SENSE)}$ is greater than $V_{IT+}$ and the $\overline{ENABLE}$ pin is low.
VCC	6	6	Supply voltage input. Connect a 1.7-V to 6.5-V supply to VCC to power the device. It is good analog design practice to place a 0.1- $\mu F$ ceramic capacitor close to this pin.

PRODUCT PREVIEW

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TPS3895ADRYR	PREVIEW	SON	DRY	6	5000	TBD	Call TI	Call TI	
TPS3895ADRYT	PREVIEW	SON	DRY	6	250	TBD	Call TI	Call TI	
TPS3895PDRYR	PREVIEW	SON	DRY	6	5000	TBD	Call TI	Call TI	
TPS3895PDRYT	PREVIEW	SON	DRY	6	250	TBD	Call TI	Call TI	
TPS3896ADRYR	PREVIEW	SON	DRY	6	5000	TBD	Call TI	Call TI	
TPS3896ADRYT	PREVIEW	SON	DRY	6	250	TBD	Call TI	Call TI	
TPS3896PDRYR	PREVIEW	SON	DRY	6	5000	TBD	Call TI	Call TI	
TPS3896PDRYT	PREVIEW	SON	DRY	6	250	TBD	Call TI	Call TI	
TPS3897ADRYR	PREVIEW	SON	DRY	6	5000	TBD	Call TI	Call TI	
TPS3897ADRYT	PREVIEW	SON	DRY	6	250	TBD	Call TI	Call TI	
TPS3897PDRYR	PREVIEW	SON	DRY	6	5000	TBD	Call TI	Call TI	
TPS3897PDRYT	PREVIEW	SON	DRY	6	250	TBD	Call TI	Call TI	
TPS3898ADRYR	PREVIEW	SON	DRY	6	5000	TBD	Call TI	Call TI	
TPS3898ADRYT	PREVIEW	SON	DRY	6	250	TBD	Call TI	Call TI	
TPS3898PDRYR	PREVIEW	SON	DRY	6	5000	TBD	Call TI	Call TI	
TPS3898PDRYT	PREVIEW	SON	DRY	6	250	TBD	Call TI	Call TI	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

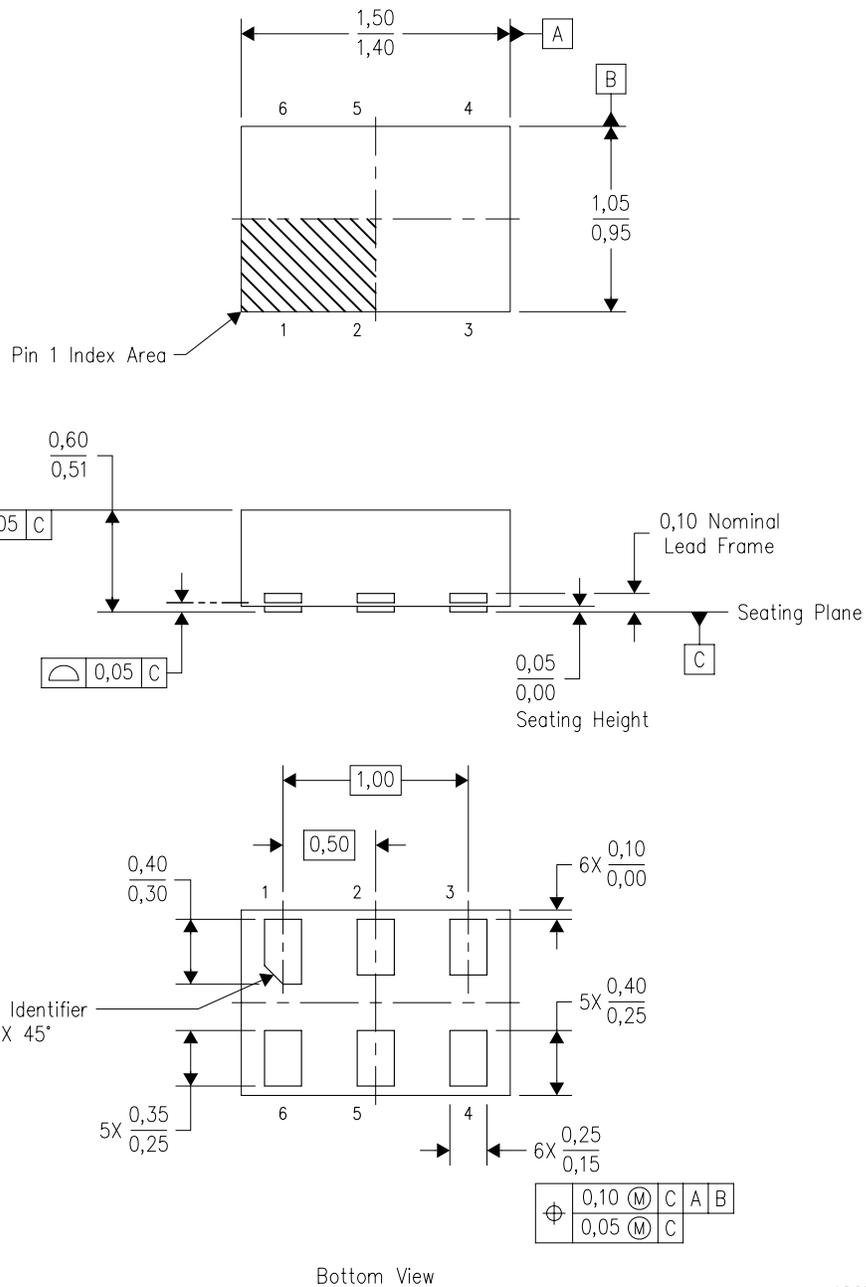
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4207181/D 12/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  - D. This package complies to JEDEC MO-287 variation UFAD.

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Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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